WHAT IS CLAIMED IS:

1. An apparatus comprising:

a buffer comprising a plurality of entries, the plurality of entries logically divided into a plurality of groups, each of the plurality of entries belonging to one of the plurality of groups;

an insert pointer indicative of which of the plurality of entries is next in the buffer to receive data;

a delete pointer indicative of which of the plurality of entries is storing oldest data in the buffer;

a plurality of first control circuits coupled to the buffer, wherein each of the plurality of first control circuits corresponds to a respective group of the plurality of groups and is configured to select an entry from the respective group for potential reading from the buffer, and wherein each of the plurality of first control circuits is configured, in the event that the delete pointer indicates a first entry in the respective group and the insert pointer wraps around the buffer and indicates a second entry in the respective group, to select the first entry if the first entry is eligible for selection; and

a second control circuit coupled to the buffer, the second control circuit configured to select a first group of the plurality of groups, wherein the entry selected from the first group by the plurality of first control circuits is the entry read from the buffer.

2. The apparatus as recited in claim 1 wherein the youngest data is written to the second

entry but the second entry is prevented from indicating that it is available for selection.

3. The apparatus as recited in claim 2 wherein the second entry includes an indication of whether or not the second entry is available for selection, and wherein the second entry is prevented from indicating that it is available by preventing assertion of the indication.

4. The apparatus as recited in claim 1 wherein each of the plurality of first control circuits and the second control circuit operate independently.

5. The apparatus as recited in claim 1 wherein each of the plurality of first control circuits and the second control circuit operate in parallel.

6. The apparatus as recited in claim 1 wherein each of the plurality of first control circuits implement a first selection mechanism, and wherein the second control circuit implements a second selection mechanism.

7. The apparatus as recited in claim 6 wherein the first selection mechanism differs from the second selection mechanism.

8. The apparatus as recited in claim 7 wherein the first selection mechanism uses the positional order of the entries in the group, and wherein the second selection mechanism uses an age vector.

9. The apparatus as recited in claim 6 wherein the first selection mechanism and the second selection mechanism are the same.

10. The apparatus as recited in claim 9 wherein the first selection mechanism and the second selection mechanism use the positional order of entries.

11. The apparatus as recited in claim 1 further comprising a plurality of multiplexors, each having inputs coupled to a respective plurality of entries forming one of the plurality of groups, and each of the plurality of first control circuits coupled to provide selection control to a respective one of the plurality of multiplexors.

12. The apparatus as recited in claim 11 further comprising a second multiplexor coupled to receive outputs of the plurality of multiplexors as inputs, wherein the second control circuit is coupled to provide selection control to the second multiplexor.

13. The apparatus as recited in claim 1 wherein a given group of the plurality of groups is eligible for selection by the second control circuit if at least one entry of the plurality of entries that is within the given group is eligible for selection.

14. A method, for a buffer comprising a plurality of entries, the plurality of entries logically divided into a plurality of groups, each of the plurality of entries belonging to one of the plurality of groups, the buffer further comprising an insert pointer indicative of which of the plurality of entries is next in the buffer to receive data and a delete pointer indicative of which of the plurality of entries is storing oldest data in the buffer, the method comprising:

selecting an entry from each group of the plurality of groups for potential reading from the buffer, wherein selecting the entry includes, in the event that the delete pointer indicates a first entry in a given group and the insert pointer wraps around the buffer and indicates a second entry in the given group, selecting the first entry if the first entry is eligible for selection; and

selecting a first group of the plurality of groups, wherein the entry selected from the first group is the entry read from the buffer.

15. The method as recited in claim 14 wherein an entry is selected from each group of the plurality of groups independently, and the first group is selected independently.

16. The method as recited in claim 15 wherein selecting the entry is performed according to a first selection mechanism, and wherein selecting the first group is performed according to a second selection mechanism.

17. The method as recited in claim 16 wherein the first selection mechanism differs from the second selection mechanism.

18. The method as recited in claim 17 wherein the first selection mechanism uses the positional order of the entries in the group, and wherein the second selection mechanism uses an age vector.

19. The method as recited in claim 16 wherein the first selection mechanism and the second selection mechanism are the same.

20. The method as recited in claim 19 wherein the first selection mechanism and the second selection mechanism use the positional order of entries.

21. The method as recited in claim 14 wherein a given group of the plurality of groups is eligible for selection if at least one entry of the plurality of entries that is within the given group is eligible for selection.

22. A processor comprising one or more circular buffers, each of the circular buffers comprising:

a buffer comprising a plurality of entries, the plurality of entries logically divided into a plurality of groups, each of the plurality of entries belonging to one

of the plurality of groups;

an insert pointer indicative of which of the plurality of entries is next in the buffer to receive data;

a delete pointer indicative of which of the plurality of entries is storing oldest data in the buffer;

a plurality of first control circuits coupled to the buffer, wherein each of the plurality of first control circuits corresponds to a respective group of the plurality of groups and is configured to select an entry from the respective group for potential reading from the buffer, and wherein each of the plurality of first control circuits is configured, in the event that the delete pointer indicates a first entry in the respective group and the insert pointer wraps around the buffer and indicates a second entry in the respective group, to select the first entry if the first entry is eligible for selection; and

a second control circuit coupled to the buffer, the second control circuit configured to select a first group of the plurality of groups, wherein the entry selected from the first group by the plurality of first control circuits is the entry read from the buffer.

23. The processor as recited in claim 22, wherein the one or more circular buffers include at least one circular buffer implemented in a scheduler, the data stored in each entry comprising operations to be executed by one or more execution cores in the processor.

24. The processor as recited in claim 22, wherein the one or more circular buffers include at least one circular buffer implemented in a retire queue.

25. The processor as recited in claim 22, wherein the one or more circular buffers include at least one circular buffer implemented as a load/store buffer storing load/store operations.